

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

CS 433: Computer System Organization

Course Information for Spring 2009

Instructor: Sarita Adve (SC 4104, sadve@illinois.edu, 217-333-8461).

Teaching Assistant: Geoffrey Levine (levine@uiuc.edu). Please refer to the course web site for office and phone number.

Administrative Assistant: Andrea Whitesell (SC 4106, whitesel@illinois.edu, 217-333-4930).

Office Hours: Sarita Adve: after class until 4:00 pm on Tuesdays and by appointment (send email to make an appointment).

TA office hours will be posted on the class web site shortly.

Web site and Newsgroup: The course home page is at <http://www.cs.uiuc.edu/class/cs433>. Most handouts, including lecture notes, homeworks, solution sets, and the lecture videos will be available here (see below). Announcements related to the class will be made on the class newsgroup, [class.cs433](mailto:cs433@uiuc.edu). The newsgroup will be the primary medium for communication between the TA and the students. It is your responsibility to check it regularly. The best way to communicate directly with Professor Adve is to send her email.

Class meeting place/time: SC 1109, Tuesday/Thursday 2:00 pm to 3:15 pm.

Pre-requisites: CS 231 or equivalent and CS232 or equivalent (specifically, Chapters 1-8 of *Computer Organization and Design: The Hardware Software Interface* by Patterson and Hennessy, 3rd edition). See the detailed section below elaborating on specific requirements from CS 232. You should also be comfortable with programming in C or C++.

Credit: 3 credits for undergraduate students. Graduate students can take the course for 3 or 4 credits. All graduate students will be required to do additional work on the assignments and possibly additional problems on the exam.

Course Material: John L. Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann Publishers Inc., **fourth edition, 2007**. The text will be supplemented with some additional material that will be provided in the lectures.

Lecture notes and handouts: Most lecture notes and handouts will be available from the course home page listed above the day before they are used in class. It is your responsibility to print them out and bring them to class.

Assignments: There will be several written assignments and possibly some machine problems. The assignments will usually be due at the beginning of class (2:00 p.m. in Illinois) on the due date. An automatic extension of 10 minutes (i.e., until 2:10 p.m. Illinois time) is given without any further request. **No further extensions for late submissions will be given in general.** For exceptional reasons, an agreement to submit an assignment late may be reached with Professor Adve. Except for unforeseen medical emergencies, the agreement must be made within 48 hours after the assignment is handed out to the class. *In all cases, you must get an email confirmation of the agreement.*

The EWS machines will be used for any machine problems. See <http://www.ews.uiuc.edu/labs>. Information about specific machines will be made available as needed.

Exams: There will be one midterm and a final exam. The midterm is tentatively scheduled for March 11th (Wednesday) from 7:00 pm to 9:00 pm in room SC 1404 (to be confirmed shortly). It will include material covered until and including March 10th (Tuesday). The final will be on May 15th (Friday) from 8:00 am to 11:00 am and will include material covered after March 10th and until the last lecture. **Requests for a conflict midterm or final**

exam should be made to the TA by email by February 3rd. Except for medical emergencies, no further requests will be granted after that time. Please indicate clearly the reason for your request. Note that a job interview is not an appropriate reason – you should schedule those around your academic schedule.

I2CS students should refer to the initial email from the TA for rules on taking exams.

Make-up classes: I will be traveling on a few Tuesdays and Thursdays for which I would like to schedule make-up classes tentatively for 2:45pm to 4pm on Feb 2, Feb 9, and March 2 (room to be announced shortly). Please send email to the TA by Jan 27 if you have a conflict for these times. The lectures will be recorded, so we will change these dates only if there are too many conflicts. The out-of-class midterm will serve to make up most of the rest of my travel. Any other required make-up will be scheduled after the mid-term.

Grading: Assignments: 20%, midterm: 40%, final: 40%.

You will be graded on an absolute scale. For graduates, the minimum score for guaranteeing a grade is as follows: A+: 95%, A : 88%, A-: 83%, B+: 78%, B : 70%, B-: 63%, C+: 58%, C : 53%, C-: 48%, D : 35%, F : 0%.

For undergraduates, the minimum score for a grade is as follows: A+: 90%, A : 83%, A-: 78%, B+: 73%, B : 65%, B-: 58%, C+: 53%, C : 48%, C-: 43%, D : 35%, F : 0%.

No D- and D+ grades will be allotted. Under exceptional circumstances, the minimum scores on some grades may be reduced, but they will not be increased.

Regrade requests: If you think you have been unfairly graded on a homework or exam, you should petition the TA or Professor Adve in writing **within a week of distribution of the graded work**. After a week, no regrade requests will be entertained.

Honor code – policies on assignments and exams: You may work with one partner for each assignment (different partners for different assignments are encouraged). Each pair of partners should submit only one set of solutions – write the names of both partners on your submission. Both partners must actively participate in the development of all the solutions. You may seek clarifications on the assignment *problems* from other students in the class as well, but you may not discuss the *solutions* with anyone other than your partner.

Exams are to be done individually. The use of the class text, class notes, class handouts, and your own assignment solutions and notes will be allowed for exams (and assignments).

Unless made available by the course staff, assignments, exams, and solution sets from previous offerings of the course or from other universities may not be used for this course. If you use such material, it is likely you will find the solutions to the problems in the assignments and the exams – we spend much time formulating the best possible set of problems and it is not possible to invent all new assignments for each course offering. Your use of such solutions will entirely defeat the goal of helping you learn the material and violate our honor code principles.

I call the above policies the honor code because I would like to largely rely on your honor to enforce them – you are the only one to lose when you cheat. I consider both giving and receiving help beyond that allowed by the honor code policies to be forms of cheating, and take a violation of the honor code very seriously. **Anyone found violating the policies will be given a failing grade on the course with no second chance. Only under exceptional circumstances will I give permission to such violators to drop the course. In all cases, a note describing the violation will be inserted in the student’s official “file.” So please read these policies very carefully.**

Details on CS 232 Pre-requisite: We assume that the student is familiar with the following material of *Computer Organization and Design: The Hardware / Software Interface* by Patterson and Hennessy, 3rd edition.

- Instruction Sets (Chapter 2)
 - Familiarity with at least one RISC instruction set (MIPS/SPARC/Alpha...)

- Addressing modes
- Arithmetic instructions
- Control instructions - jump, conditional branch
- Procedure calls and returns
- Basics of Computer Arithmetic (Chapter 3)
- Basic Understanding for Assessing Performance (Chapter 4)
- Simple processor implementation (Chapter 5)
 - Data and control paths for single and multiple cycle implementations
 - Microprogrammed vs. hardwired control
 - Basic exception or interrupt handling
- Basic pipelined implementation (Chapter 6)
 - Structural, data, and control hazards
- Memory hierarchies – Caches and Virtual Memory (Chapter 7)
 - Concept of locality
 - Concepts of miss vs. hit, miss and hit ratios, block or line, page, page fault, address translation, purpose of a translation lookaside buffer (TLB)
 - On a miss, where to place a block (associativity), which block to replace (LRU, random, etc. replacement policy), how to find a block (page index, tags, etc.), what to do on a write (writethrough vs. writeback)
- Basics of I/O – disks and buses (Chapter 8)

Topics for this course

- Introduction – review of fundamental performance issues, power and reliability, cost vs. price, basic pipeline structure
- Instruction level parallelism – hardware and software techniques (e.g., dynamic scheduling, superscalar, static and dynamic branch prediction, VLIW, loop unrolling).
- Memory hierarchy – advanced concepts in caches (e.g., prefetching, lockup-free caches, and multi-level caches), main memory, and virtual memory.
- Multiprocessors/multicore – overview of different models, cache coherence with shared-memory systems/multicore (snoopy and directory solutions), synchronization.
- Storage systems, I/O
- Recent advances in architecture and future challenges – *depending on available time*