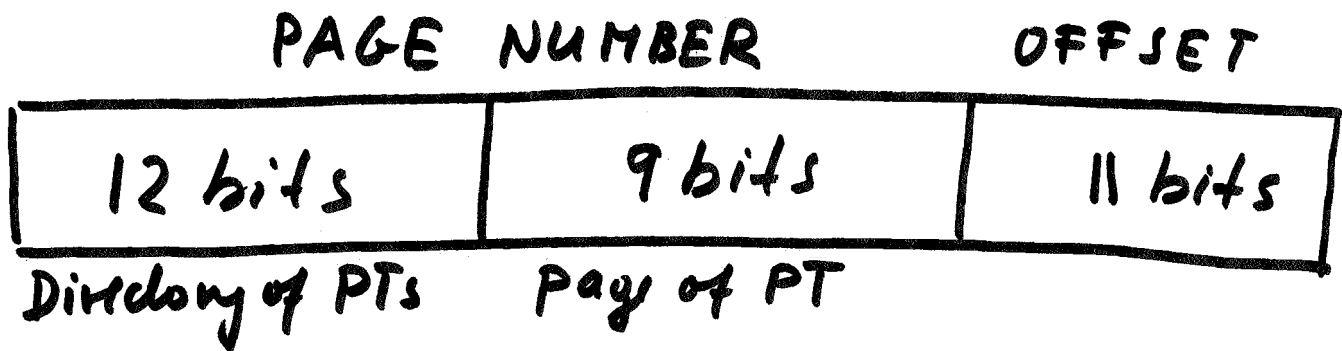


## Example A:

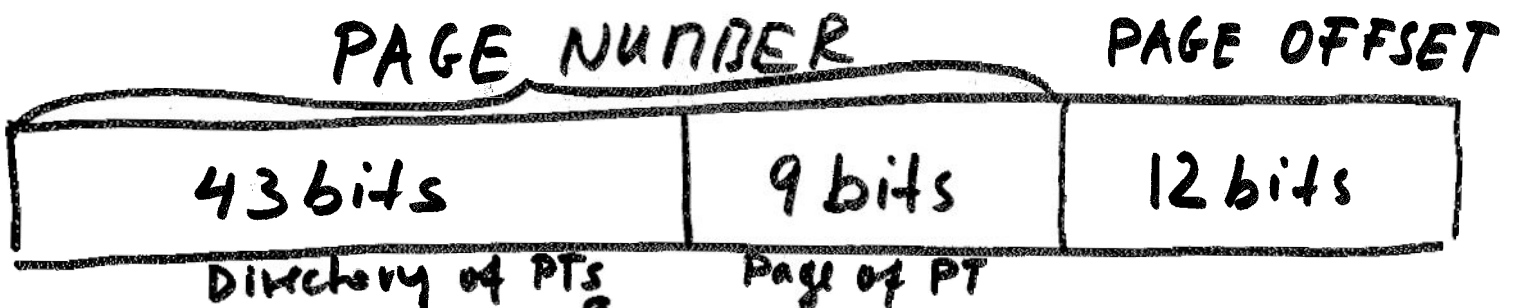
- 32-bit Architecture  $\Rightarrow 32:8 = 4$  Byte Address
- Assume  $2K = 2048$  Bytes =  $2^{11}$  Bytes PAGE SIZE



- $\rightarrow 2048:4 = 512 = 2^9$  entries of 4 Byte Addresses
- $\rightarrow 32-20 = 12$  bits for directory of Page Tables

## Example B:

- Assume 64-bit Architecture  $\Rightarrow 64:8 = 8$  Bytes per Address  
(1 Byte = 8 bits)
- Assume  $4K = 4096 = 2^{12}$  Bytes PAGE SIZE



- $4096:8 = 512 = 2^9$  entries of 8 Byte Addresses in a Page of PT
- $\downarrow$   
size of Address

$64 - (9 + 12) = 43$  bits for directory of Page Tables